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EXAMINER	
DANIELS, ANTHONY J	
ART UNIT	**PAPER NUMBER**
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/993,917	STARK, MOSHE	
	Examiner	Art Unit	
	Anthony J. Daniels	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment, filed 4/2/2007, has been entered and made of record. Claims 1-46 are pending in the application.

Response to Arguments

1. Applicant's arguments regarding Pain et al. and the independent claims have been fully considered but they are not persuasive.

In a closer examination of the reference, Pain et al. discloses the newly added features of claim 1. Applicant asserts, "...Pain's circuitry discloses a differential readout of charges, and so does not contemplate a capacitor that is configured to sum charges from at least two units cells..." The examiner respectfully disagrees with this statement. The differential readout of charges concerns correlated double sampling. The amplifier "A" in Figure 2-1 differentially integrates the charges. Pain et al. will be considered in more detail in the rejections that follow.

2. All other arguments with respect to independent claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claims 45 and 46 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In claims 45 and 46, the language, "...each amplifier selector receives output from at least three unit cells...", is not supported by the specification. In Figure 8, the amplifier selectors only have three inputs for only three unit cells. Three unit cells are supported. At least three unit cells are not.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1,12,23-27 and 34-38 rejected under 35 U.S.C. 103(a) as being unpatentable over Pain et al. (US # 6,801,258).

As to claim **1**, Pain et al. teaches an active pixel image sensor (Figure 1, APS imager "10") comprising: a plurality of unit cells, each adapted to generate charge in response to photons incident thereon (Figure 1, pixels "17"); and array elements (Figure 2-1, among other elements, column control "50") adapted to sum charge from least two unit cells at a focal plane of said image sensor (Col. 2, Lines 20 and 21), wherein said array elements comprise: a plurality

of charge integration capacitors (Figure 2-1, capacitor CLS; Col. 3, Lines 4-6 and 41-53; Col. 2, Lines 33-36), each charge integration capacitor associated with an amplifier (Figure 2-1, op-amp "A") and configured to sum charges from at least two unit cells (Col. 3, Lines 4-6 and 41-53; Col. 2, Lines 33-36). Although Pain et al. does not state it explicitly, **Official Notice** is taken that direct injection unit cells are well known and expected in the art. One of ordinary skill in the art would have motivated to implement direct injection unit cells as the unit cells in Sauer et al., because direct injection unit cells mitigate blooming effects in CMOS sensors.

Since Applicant has failed to timely traverse the old and well known statement above, it is now taken as admitted prior art. See MPEP 2144.03 (c).

As to claim **12**, Pain et al. teaches an active pixel image sensor (Figure 1, APS imager "10") comprising: a plurality of unit cells, each adapted to generate charge in response to photons incident thereon (Figure 1, pixels "17"); and array elements (Figure 2-1, among other elements, column control "50") adapted to change a resolution of the output of said image sensor at a focal plane of said image sensor (Col. 2, Lines 13-18) by summing the charge generated by at least two unit cells of said plurality of unit cells (Col. 2, Lines 20 and 21), wherein said array elements comprise: a plurality of charge integration capacitors (Figure 2-1, capacitor CLS; Col. 3, Lines 4-6 and 41-53; Col. 2, Lines 33-36), each charge integration capacitor associated with an amplifier (Figure 2, op-amp "A") and configured to sum charges from at least two unit cells (Col. 3, Lines 4-6 and 41-53; Col. 2, Lines 33-36). Although Pain et al. does not state it explicitly, **Official Notice** is taken that direct injection unit cells are well known and expected in the art. One of ordinary skill in the art would have motivated to implement direct injection unit

cells as the unit cells in Sauer et al., because direct injection unit cells mitigate blooming effects in CMOS sensors.

Since Applicant has failed to timely traverse the old and well known statement above, it is now taken as admitted prior art. See MPEP 2144.03 (c).

As to claim **23**, claim 23 is a method claim corresponding to apparatus claim 1. Therefore, method claim 23 is analyzed and rejected as previously discussed with respect to the apparatus claim 1.

As to claim **24**, Pain et al. teaches a method according to claim 23 and wherein said summing comprises: activating charge transfer transistors (Figure 2-1, ROW) of one or more lines of unit cells (Col. 2, Lines 30-32); activating one or more columns of unit cells (Col. 3, Lines 55-62); and combining the charge transferred by activated charge transfer transistors of said activated columns (Col. 3, Lines 40-62).

As to claim **25**, Pain et al. teaches a method according to claim 23 wherein said summing comprises activating at least two adjacent lines and selecting one column thereby to combine charge from the corresponding unit cells in adjacent lines (Col. 2, Lines 18-20; *{n=2, m=1}*).

As to claim **26**, Pain et al. teaches a method according to claim 23 and wherein said summing comprises activating one line and combining charge of at least two columns thereby to combine charge from at least two unit cells in adjacent columns (Col. 2, Lines 18-20; *{n=1, m=2}*).

As to claim **27**, Pain et al. teaches a method according to claim 23 and wherein said summing comprises activating U adjacent lines and combining charge of V columns thereby to combine charge from UxV unit cells in a UxV block (Col. 2, Lines 18-20).

As to claim **34**, claim 34 is a method claim corresponding to apparatus claim 12. Therefore, method claim 34 is analyzed and rejected as previously discussed with respect to the apparatus claim 12.

As to claims **35-38**, the limitations in claims 35-38 can be found in claims 24-27, respectively. Therefore, claims 35-38 are analyzed and rejected as previously discussed with respect to claim 24-27, respectively.

2. Claims 2-5,13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pain et al. (US # 6,801,258) in view of Sauer et al. (US # 5,973,311).

As to claim **2**, Pain et al. teaches an image sensor according to claim 1, wherein: each of said unit cells comprises: a charge transfer transistor adapted to transfer charge from their said each unit cell when activated (Figure 2-1, ROW transistor); and said array elements further comprise: a line decoder (Figure 1, sensor row decoder "20") adapted to activate the charge transfer transistors of one or more lines of unit cells (Col. 2, Lines 25 and 26); and a column selector (Figure 1, column select logic "60" and global integrator "70") adapted to activate one or more columns of unit cells and to combine the charge transferred by activated charge transfer transistors of said activated columns (Col. 3, Lines 57-60). The claim differs from Pain et al. in that it further requires that each unit cell include a unit cell charge integration capacitor capable of storing charge generated in response to the photons.

In the same field of endeavor, Sauer et al. teaches an CMOS image sensor comprises a plurality of unit cells (Figure 4). Each unit cell includes a charge storage capacitor (Figure 2, capacitor "C11") connected to a photodiode (Figure 2, photodiode "P11") and charge transfer

transistor (Figure 2, transistor "TR11"). In light of the teaching of Sauer et al., it would have been obvious to one of ordinary skill in the art to include the capacitor in the pixel of Pain et al., because an artisan of ordinary skill in the art would recognize that this would allow for an increased maximum charge handling capacity of the pixel (see Sauer et al., Col. 5, Lines 9-21).

As to claim **3**, Pain et al., as modified by Sauer et al., teaches an image sensor according to claim 2 and wherein said array elements comprise adjacent line means adapted to indicate to said line decoder to activate at least two adjacent lines and to said column selector to select one column thereby to combine charge from the corresponding unit cells in adjacent lines (see Pain et al., Figure 1, sensor row decoder "20"; Col. 2, Lines 18-20).

As to claim **4**, Pain et al., as modified by Sauer et al., an image sensor according to claim 2 and wherein said array elements comprise adjacent column means adapted to indicate to said line decoder to activate one line and to said column selector to combine charge of at least two columns thereby to combine charge from at least two unit cells in adjacent columns (see Pain et al., Figure 1, column select logic "60"; Col. 2, Lines 18-20).

As to claim **5**, Pain et al., as modified by Sauer et al., teaches an image sensor according to claim 2 and wherein said array elements comprise block means adapted to indicate to said line decoder to activate U adjacent lines and to said column selector to combine charge of V columns thereby to combine charge from UxV unit cells in a UxV block (see Pain et al., Col. 2, Lines 18-20).

As to claims **13-16**, the limitations of claims 13-16 can be found in claims 2-5, respectively. Therefore, claims 13-16 are analyzed and rejected as previously discussed with respect to claims 2-5, respectively.

3. Claims 6-11 and 17-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pain et al. (US # 6,801,258) in view of Sauer et al. (US # 5,973,311) and further in view of Nishida et al. (US # 4,996,600).

As to claim **6**, Pain et al., as modified by Sauer et al., teaches an image sensor according to claim 3. The claim differs from Pain, as modified by Sauer et al., in that it further requires interlace means adapted to produce video output from said image sensor in an interlace mode.

In the same field of endeavor, Nishida et al. teaches an interlace means adapted to produce video output from said image sensor (Col. 3, Lines 26-34) in an interlace mode (Figure 6A and Figure 6B). In light of the teaching of Nishida et al. it would have been obvious to one of ordinary skill in the art at the time the invention was made to include interlace means adapted to produce video output from said image sensor in an interlace mode in the sensor of Pain et al. Such a means would allow for a sufficiently large charge with little noise to be obtained, increased dynamic range and; consequently, high-quality reproduced images, with reduced residual images, can be obtained (see Nishida et al., Col. 2, Lines 43-48).

As to claim **7**, Pain et al., as modified by Sauer et al. and Nishida et al., teaches an image sensor according to claim 6 and wherein said interlace means comprises means adapted to activate said adjacent line means to combine charge of pairs of unit cells in adjacent lines beginning with the odd lines adapted to an odd field output and of adjacent lines beginning with the even lines adapted to an even field output (see Nishida et al., Figure 6A and Figure 6B).

Note the interchangeability of rows and columns in the Pain et al. reference. Also note Col. 7, Lines 34-38 in Nishida et al. when considering 4,996,600 as prior art.

As to claim **8**, Pain et al., as modified by Sauer et al., teaches an image sensor according to claim 4. The claim differs from Pain, as modified by Sauer et al., in that it further requires intercolumn means adapted to produce video output from said image sensor in an intercolumn mode.

In the same field of endeavor, Nishida et al. teaches an intercolumn means adapted to produce video output from said image sensor (Col. 3, Lines 26-34) in an intercolumn mode (Figure 6A and Figure 6B). In light of the teaching of Nishida et al. it would have been obvious to one of ordinary skill in the art at the time the invention was made to include intercolumn means adapted to produce video output from said image sensor in an intercolumn mode in the sensor of Pain et al. Such a means would allow for a sufficiently large charge with little noise to be obtained, increased dynamic range and; consequently, high-quality reproduced images, with reduced residual images, can be obtained (see Nishida et al., Col. 2, Lines 43-48).

As to claim **9**, Pain et al., as modified by Sauer et al. and Nishida et al., teaches an image sensor according to claim 8 and wherein said intercolumn means comprises means adapted to activate said adjacent column means to combine charge of pairs of adjacent columns beginning with the odd columns adapted to an odd field output and of adjacent columns beginning with the even columns adapted to an even field output (see Nishida et al., Figure 6A and Figure 6B).

As to claim **10**, Pain et al., as modified by Sauer et al., teaches an image sensor according to claim 5. The claim differs from Pain, as modified by Sauer et al., in that it further requires block interlace means adapted to produce video output from said image sensor in a block interlace mode.

In the same field of endeavor, Nishida et al. teaches a block interlace means for generating a 2x2 block interlace readout (Figure 1; Col. 3, Line 38 – Col. 4, Line 7). In light of the teaching of Nishida et al. it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the block interlace means adapted to produce video output from said image sensor in a block interlace mode in the sensor of Pain et al. Such a means would allow for a sufficiently large charge with little noise to be obtained, increased dynamic range and; consequently, high-quality reproduced images, with reduced residual images, can be obtained (see Nishida et al., Col. 2, Lines 43-48).

As to claim **11**, Pain et al., as modified Sauer et al. and Nishida et al., teaches an image sensor according to claim 10 and wherein said block interlace means comprises means adapted to activate said block means to combine charge of 2x2 blocks wherein the blocks of an odd field output begin with the block whose upper left-hand unit cell is in the first column, first line and wherein the blocks of an even field output begin with the block whose upper left-hand unit cell is in the second column, second line (see Nishida et al., Figure 1).

As to claims **17-22**, the limitations of claims 17-22 can be found in claims 6-11, respectively. Therefore, claims 17-22 are analyzed and rejected as previously discussed with respect to claims 6-11, respectively.

4. Claims 28-33 and 39-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pain et al. (US # 6,801,258) in view of Nishida et al. (US # 4,996,600).

As to claim **28**, Pain et al. teaches a method according to claim 25. The claim differs from Pain et al. in that it further requires producing video output from said image sensor in an interlace mode.

In the same field of endeavor, Nishida et al. teaches an interlace means adapted to produce video output from said image sensor (Col. 3, Lines 26-34) in an interlace mode (Figure 6A and Figure 6B). In light of the teaching of Nishida et al. it would have been obvious to one of ordinary skill in the art at the time the invention was made to include interlace means adapted to produce video output from said image sensor in an interlace mode in the sensor of Pain et al. Such a means would allow for a sufficiently large charge with little noise to be obtained, increased dynamic range and; consequently, high-quality reproduced images, with reduced residual images, can be obtained (see Nishida et al., Col. 2, Lines 43-48).

As to claim **29**, Pain et al., as modified by Nishida et al., teaches a method according to claim 28 and wherein said producing comprises combining charge of pairs of unit cells in adjacent lines beginning with the odd lines for an odd field output and of adjacent lines beginning with the even lines for an even field output (see Nishida et al., Figure 6A and Figure 6B).

As to claim **30**, Pain et al. teaches a method according to claim 26. The claim differs from Pain et al. in that it further requires producing video output from said image sensor in an intercolumn mode.

In the same field of endeavor, Nishida et al. teaches an intercolumn means adapted to produce video output from said image sensor (Col. 3, Lines 26-34) in an intercolumn mode (Figure 6A and Figure 6B). In light of the teaching of Nishida et al. it would have been obvious

to one of ordinary skill in the art at the time the invention was made to include intercolumn means adapted to produce video output from said image sensor in an intercolumn mode in the sensor of Pain et al. Such a means would allow for a sufficiently large charge with little noise to be obtained, increased dynamic range and; consequently, high-quality reproduced images, with reduced residual images, can be obtained (see Nishida et al., Col. 2, Lines 43-48).

As to claim **31**, Pain et al., as modified by Nishida et al., teaches a method according to claim 30 and wherein said producing comprises combining charge of pairs of adjacent columns beginning with the odd columns for an odd field output and of adjacent columns beginning with the even columns for an even field output (see Nishida et al., Figure 6A and Figure 6B).

Note the interchangeability of rows and columns in the Pain et al. reference. Also note Col. 7, Lines 34-38 in Nishida et al. when considering 4,996,600 as prior art.

As to claim **32**, Pain et al. teaches a method according to claim 31. The claim differs from Pain et al. in that it further requires producing video output from said image sensor in a block interlace mode.

In the same field of endeavor, Nishida et al. teaches a block interlace means for generating a 2x2 block interlace readout (Figure 1; Col. 3, Line 38 – Col. 4, Line 7). In light of the teaching of Nishida et al. it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the block interlace means adapted to produce video output from said image sensor in a block interlace mode in the sensor of Pain et al. Such a means would allow for a sufficiently large charge with little noise to be obtained, increased dynamic range and; consequently, high-quality reproduced images, with reduced residual images, can be obtained (see Nishida et al., Col. 2, Lines 43-48).

As to claim **33**, Pain et al., as modified by Nishida et al., teaches a method according to claim 32 and wherein said producing comprises combining charge of 2x2 blocks wherein the blocks of an odd field output begin with the block whose upper left-hand unit cell is in the first column, first line and wherein the blocks of an even field output begin with the block whose upper left-hand unit cell is in the second column, second line (see Nishida et al., Figure 1).

As to claims **39-44**, the limitations of claims 39-44 can be found in claims 28-33, respectively. Therefore, claims 39-44 are analyzed and rejected as previously discussed with respect to claims 28-33, respectively.

Conclusion

1. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony J. Daniels whose telephone number is (571) 272-7362. The examiner can normally be reached on 8:00 A.M. - 5:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc-Yen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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